Atom-Probe Tomography of Semiconductor Materials and Device Structures

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Abstract

The development of laser-assisted atom-probe tomography (APT) analysis and new sample preparation approaches have led to significant advances in the characterization of semiconductor materials and device structures by APT. The high chemical sensitivity and three-dimensional spatial resolution of APT makes it uniquely capable of addressing challenges resulting from the continued shrinking of semiconductor device dimensions, the integration of new materials and interfaces, and the optimization of evolving fabrication processes. Particularly pressing concerns include the variability in device performance due to discrete impurity atom distributions, the phase and interface stability in contacts and gate dielectrics, and the validation of simulations of impurity diffusion. This overview of APT of semiconductors features research on metal-silicide contact formation and phase control, silicon field-effect transistors, and silicon and germanium nanowires. Work on silicide contacts to silicon is reviewed to demonstrate impurity characterization in small volumes and indicate how APT can facilitate defect mitigation and process optimization. Impurity contour analysis of a pFET semiconductor demonstrates the site-specificity that is achievable with current APTs and highlights complex device challenges that can be uniquely addressed. Finally, research on semiconducting nanowires and nanowire heterostructures demonstrates the potential for analysis of materials derived from bottom-up synthesis methods.

Metrology Challenges in Highly Scaled Semiconductors

Materials characterization of semiconductors plays an essential role in the steady improvements in semiconductor technology performance and costs. As device dimensions shrink, impurity atom diffusion is strongly affected by interface proximity and segregation. The structural three-dimensional effects on diffusion and impurity activation cannot be characterized by many conventional characterization tools. Secondary ion mass spectroscopy (SIMS) and transmission electron microscopy (TEM) have been the main sources of information on impurity diffusion and materials structure, respectively. Shrinking device dimensions have, however, long surpassed the lateral resolution of SIMS, so diffusion studies are limited to planar structures. TEM-based techniques, including electron energy loss spectroscopy (EELS) and x-ray fluorescence, have a spatial resolution comparable to the probe diameter of 1 nm. While this spatial resolution is suitable for small geometry device analysis, sensitivity is limited for impurities; arsenic can be detected to 5×10^{20} cm^{-3} but not at the typical junction concentrations of ~5×10^{18} cm^{-3}. In contrast, the combined high sensitivity (~5×10^{17} cm^{-3} or 10 appm) and subnanometer-scale spatial resolution of atom-probe tomography (APT) suggest an important role for it in future device characterization.[1,2] APT measurements also have the potential to greatly improve modeling of processes; the availability of precise and accurate information at the atomic scale in 3D is extremely useful for calibrating and validating models of impurity atom implantation and diffusion.

As decreasing device dimensions necessitate the industry to move from planar silicon device technology to more complex geometrical designs such as multigate transistors, fin-shaped field-effect transistors, and tri-gate transistors, the challenge of ensuring a specific impurity distribution, and thereby a well-defined charge distribution, increases greatly. To enable APT to analyze these complex structures, a combination of top-down and bottom-up sample preparation approaches have been developed, as illustrated in Figure 1. The availability of dual-beam focused ion beam (FIB) microscopy-based sample preparation methods[3,4] has enabled site-specific characterization of portions of the device structure under consideration (Figure 1c and 1d). The development of novel bottom-up approaches to nanowire growth[29] has enabled the analysis of nanowire specimens grown in place (Figure 1b).

The TEM image of the device in cross section (Figure 1c) shows the materials diversity in a silicon device as revealed by the contrast differences. If the APT microtip is composed of regions with differing evaporative properties, such as metal, oxide, and nitride dielectrics, the surface will field evaporate, preferentially leading to changes in surface topography. Small changes in the radius of curvature of a microtip can distort the positioning of atoms in the 3D reconstruction causing length-scale errors.[2] To alleviate this problem, the device is stripped back to the semiconductor silicon features, removing the silicon oxide and nitride layers, in particular, and refilling the space with a conformal chemical vapor deposition (CVD) coating of silicon, Figure 1d. When formed into a microtip, this predominantly silicon sample will evaporate smoothly and enable accurate 3D reconstructions of the device structure. We note that the dual-beam FIB microscope must have sufficient imaging resolution to place the encapsulated device in the center of the sharp tip with less than 20 nm tolerance for placement error. The process involves cutting a wedge from the silicon wafer that includes the device, mounting this section on an analysis post, and then

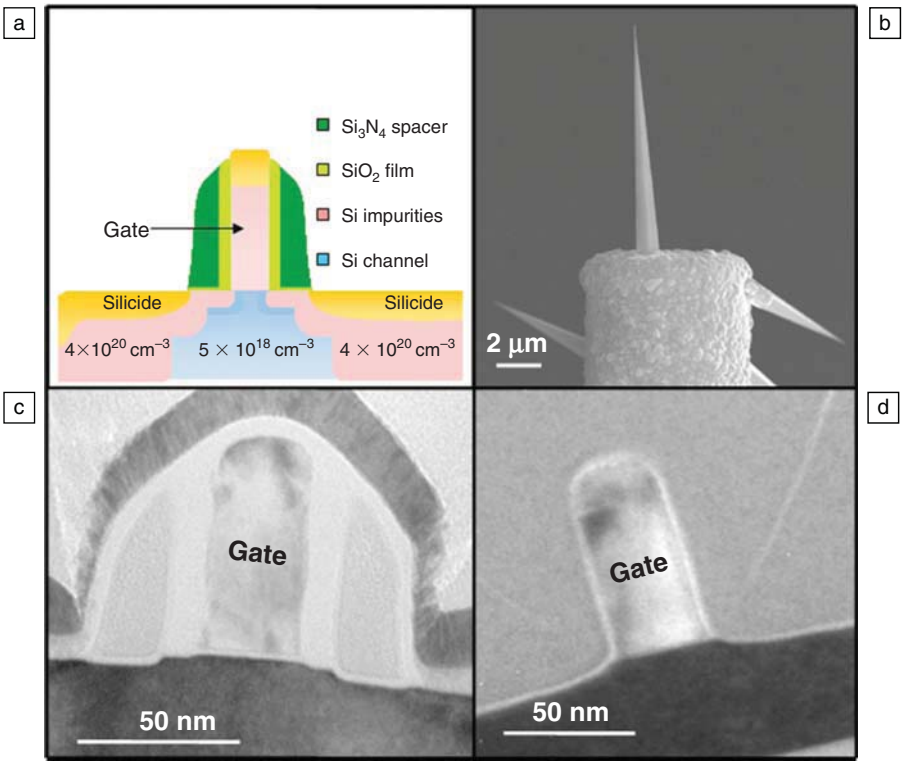

Figure 1. (a) Schematic illustrating typical doping concentrations in different regions of a transistor device. (b) Silicon nanowires grown in place over silicon microposts for atom-probe tomography studies. (c) Transmission electron microscopy (TEM) image of a pFET in cross section with spacers illustrating the complex materials combinations in a typical device. (d) TEM image of a pFET device after etching treatments to remove the dielectric spacers and subsequent backfill using chemical vapor deposition silicon to ensure uniform and nonpreferential field evaporation.

forming a sharp microtip with the device at its center by sputtering away material with a low-energy Ga^+ ion beam. The region of the surface that is damaged by the ion beam is visible in the reconstruction and is therefore readily discarded from the subsequent analysis. By enabling high spatial resolution composition measurements in 3D in thin films and complex device structures, these and other techniques have opened up important opportunities for the design of future semiconductor devices, integration of new material systems, and optimization of the fabrication process flow to control defects and variability. Areas of particular interest, which will be addressed in this article, are the transition metal distribution in silicide contacts, impurity contour analysis in the source-drain extension regions under the gate, and the characterization of nanowire heterostructures.

Silicide Contacts to Silicon

As semiconductor device dimensions shrink with every technology generation, new silicide source-drain contacts (Figure 1a) have been developed. Previously used Ti- and Co-silicides have now given way to Ni-based silicides primarily due to their low resistivity, lower temperature of formation, and lower silicon consumption.[5] It is important to ensure the formation and retention of the low resistivity phase among the various possible silicide phases at the end of the device fabrication process. In the case of Ni-silicides, six different stable phases have been reported at room temperature. Often these phase changes deviate from the expected equilibrium phase formation sequences and are dependent on a host of process parameters, such as impurity type and fluence, substrate type, metal thickness, surface preparation, and annealing conditions, thus making fabrication of reliable contacts challenging. However, materials analysis is difficult at this small length scale. X-ray diffraction is limited due to the small volume available. TEM has compositional analysis capability at the device dimensions, but of the significant impurities, only arsenic is detectable below 1 at.%. The As concentration in the doped silicon under the Ni during silicide formation is near the As solubility limit; when this Si is consumed in the silicide formation, the rejected As accumulates at grain boundaries or interfaces. For microelectronic device optimization, this segregation needs to be minimized to retain the silicon conductivity in the contact region. High-precision characterization using APT gives us an opportunity to study not only the phase formation and evolution but also 3D impurity distributions, interface chemical roughness, and diffusion issues, all of which are relevant to the fabrication of low-resistivity contacts.

NiSi is the low resistivity phase of interest for present day contact applications in complementary metal oxide semiconductor (CMOS) field-effect transistors. The main drawbacks of this system include (1) agglomeration of the desired NiSi phase, which causes an increase in the resistivity, and (2) formation of the higher resistivity $NiSi_2$ phase during silicide processing. The addition of transition metal elements such as Pd, Pt, or Rh, however, has been shown to reduce the agglomeration of thin NiSi films and increase the formation temperature of $NiSi_2$.[6,7] Using local-electrode atom-probe (LEAP) tomography, Kim et al.[8] explained the enhanced resistance to agglomeration exhibited by Pd-doped films. Figure 2b displays a proximity histogram (or proxigram) for a Ni (5 at.% Pd) thin film on Si(100) subjected to rapid thermal annealing to form a monosilicide phase followed by a post-anneal treatment to simulate the back-end-of-line process. A proxigram is a 3D nonlinear concentration profile created by calculating the average concentration within a defined voxel size as we propagate the topological shape of the isoconcentration surface in the film.[9] The segregation of Pd at the NiSi/Si interface, as illustrated by the peak in Pd concentration, Figure 2b, is driven by a decrease in the interfacial Gibbs free energy. This leads to a concomitant decrease in the driving force for agglomeration of the monosilicide film and results in a stable silicide film resistant to morphological degradation during subsequent processing at elevated temperatures. Similarly, Ronsheim et al.[10] observed the segregation of Pt at the NiSi/Si heterophase interface in TiN-capped Ni(Pt)Si film on *n*-type Si, thereby establishing interfacial segregation of transition metal elements as the predominant reason for enhanced resistance to agglomeration. Figure 3 exhibits segregation of both Pt and As dopants at the NiSi/Si interface by both TEM spectroscopy and APT.

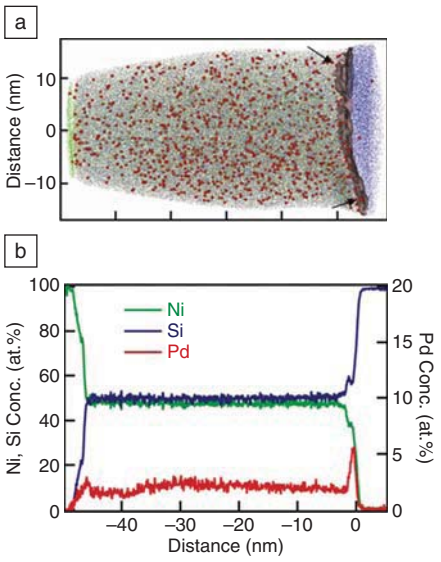

Figure 2. (a) Two-dimensional projection of the full 3D reconstruction of local electrode atom-probe tomography showing the distribution of elements (colored points) and the isoconcentration surface (shaded sheet indicated by arrows) that defines the heterophase interface. Ni, Si, and Pd atoms are shown in green, blue, and red, respectively. Pd atoms are enlarged, and only 10% of the Si atoms are shown for clarity. Within the NiSi phase, the Pd is seen to be distributed uniformly. The Ni atoms on the left are from a protective capping layer. (b) Proxigram (proximity histogram) displaying the concentrations of Ni, Si, and Pd versus film depth. Concentrations were calculated for a series of isoconcentration surfaces moving into the thin film; the NiSi/Si heterophase interface provides an example of an isoconcentration surface. Reprinted with permission from Reference 8. ©2007, American Institute of Physics.

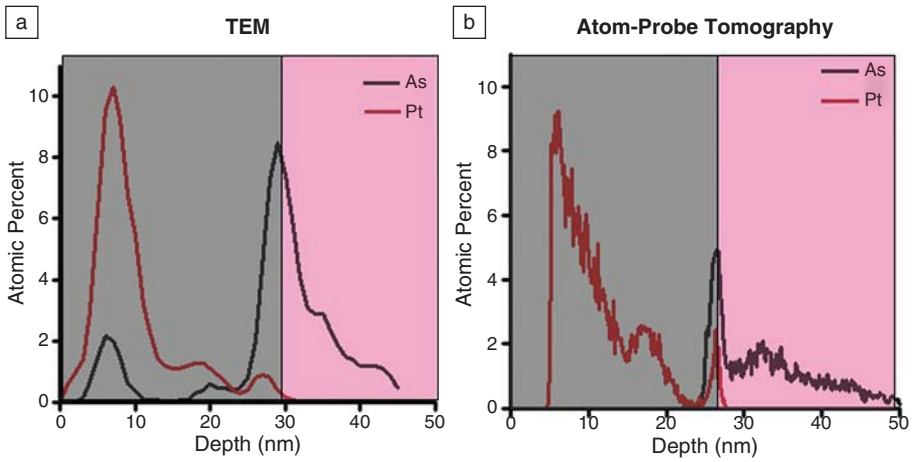

Figure 3. One-dimensional composition profiles across the NiSi/Si interface showing the segregation of Pt and As at this interface by (a) energy dispersive x-ray analysis and (b) atom-probe tomography. The gray and pink shaded regions represent the silicide and silicon substrate portions of the thin film, respectively. TEM, transmission electron microscopy. Adapted from Reference 10.

The 1D compositional line analysis using TEM energy-dispersive spectroscopy with 1–2 nm spatial resolution confirms the observation by APT.

Additionally, Pt has also been reported[11–13] to segregate to the interphase boundary between Ni_2Si and NiSi and also to the $Ni_{1-x}Pt_x/Ni_2Si$ interface via a snowplow effect. Insights into the interplay between silicide phase formation and Pt interdiffusion have led to greater understanding of phase stability in this complex materials system. Adusumilli et al.[14,15] have reported evidence of short-circuit diffusion via the grain boundaries of the NiSi phase after rapid thermal annealing at 420°C for 5 s, providing valuable insights into the kinetics of the diffusion processes during the silicidation process. The presence of high-diffusivity paths via the grain boundaries and the diffusion of Pt to the NiSi/Si heterophase interface for these short timescales raise important questions about the impact of Pt on NiSi grain growth and grain morphology. Akutsu et al.[16] have reported a smaller NiSi grain size and modification of the grain morphology in the presence of Pt, probably due to grain boundary pinning by Pt. The smaller grain size in NiSi is preferable due to the increase in resistance to agglomeration and thereby the thermal stability of the thin film. Studies on the effect of Pt addition on the microstructure and grain morphology of NiSi have been uniquely enabled by APT.

APT has been utilized in conjunction with other complementary tools, such as TEM, to study phase formation and stabilization, interface chemical roughness, segregation at the silicide-silicon interface, and metal diffusion in these novel contact structures. This is an important example of how insights provided by APT measurements are being utilized for the development of new silicide materials, as well as the optimization of the fabrication process to control defects and produce reliable contacts to silicon. Most of the research in this section was performed on large-area thin-film structures; the next section illustrates the site-specific nature of APT measurements for impurity contour analysis of a pFET semiconductor device made possible by the application of a dual-beam FIB microscope for sample preparation.

Silicon Device Analysis with APT

For the current generation of planar transistors, the lateral diffusion of the source-drain extension under the gate edge is of particular interest (Figure 1a). A silicon device for the 32-nm technology will typically have a 30 nm × 50 nm gate bounded on two sides by silicon oxynitride and on the other two sides by nickel silicide contacts, with silicon oxide and silicon nitride film layers to separate the conductive NiSi contacts from the gate contact. This asymmetric structure and impurity atom distribution creates electrical charge distributions unique to the compositions at corners and interfaces that have been difficult to characterize. Measurement of this impurity diffusion for several annealing conditions is needed to accurately model the impurity distribution. As noted, TEM has sufficient analytical resolution for current technology, but its sensitivity to impurity concentrations is limited to 5×10^{20} cm^{-3} for favorable elements such as arsenic and is over 1×10^{21} cm^{-3} in important cases such as B in Si. APT has the requisite resolution and sensitivity to characterize the dopant atom concentration and diffusion and provide feedback to the designer for device improvements. Using a relatively simple sample preparation procedure, a Si device can be analyzed using APT, with a sensitivity of 1×10^{19} cm^{-3}. Although electron holography[17] and scanning probe methods[18] can indirectly measure carrier concentrations, APT is the only technique capable of directly measuring impurity concentration fluctuations at the device dimensions.

To demonstrate the application of APT, we consider a mature 65 nm SOI substrate process, where gate lengths are near 45 nm, and the gate dielectric is a simple Si oxynitride. The test structure—a pFET device—is designed to determine dopant diffusion under the spacers by measuring the capacitance between the gate and source/drain. The combination of conductive and dielectric layers around the gate and the complex geometry make the sample preparation process somewhat more involved. The sample is prepared for a cross-sectional APT analysis, with the long axis of the microtip oriented parallel to the surface so the gate cross section is presented to the evaporating microtip face.[19] Spacer silicon nitride material was partially removed with wet chemical etching and then capped with CVD silicon (Figure 1d) prior to the tip shaping. Figure 4 is an image of the reconstructed pFET atoms: silicon in gray, oxygen in red, and boron in blue. Silicon oxide is seen surrounding the gate polysilicon, and the buried oxide is underneath the device channel. The B concentration can be summed along the width of the device (into the figure) and used to generate a concentration profile from the contact area through the gate channel.[19] Boron 1D profiles can thus be extracted (not shown here) from the 3D reconstruction and correlated to electrical device parameters, including drive current and resistance. Difficult device design issues, such as the device resistance between source and drain to the channel, can now be attacked with APT experiments to measure diffusion in this 3D structural element.

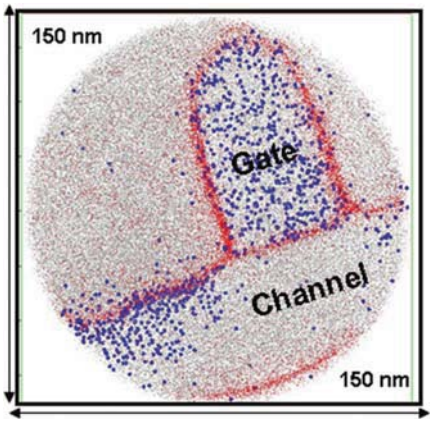

Figure 4. Two-dimensional image from an atom-probe reconstruction of boron impurities in a silicon transistor in cross section, with Si, O, and B represented by gray dots, red dots, and blues spheres, respectively. Adapted from Reference 19.

Semiconductor Nanowires

Another approach to the scaling of channel widths to smaller dimensions relies on nanowires whose diameters are defined by nanoscale catalysts.[21] Catalyst-mediated bottom-up growth is suitable for a range of next-generation materials, including the most common Group IV, III–V, and II–VI semiconductors.[20] In addition, nanowires provide a wealth of opportunities for new science in low-dimensional materials and are a platform for nanotechnologies beyond CMOS devices.[20,22]

The small diameters and extreme aspect ratios of nanowires complicate the measurement of their composition. While scanning transmission electron microscopy (STEM)-based techniques can be used to measure the composition of individual wires, there are significant limitations in sensitivity that are impurity-dependent. APT provides distinct advantages for addressing a number of important measurement challenges. First, dopant distribution analysis across and along a nanowire requires single-atom sensitivity and subnanometer spatial resolution that only APT can provide. High-resolution SIMS has been performed on micron-diameter wires, but SIMS is not presently suitable for nanowires due to limitations on resolution.[23] Second, composition fluctuations that are small in both magnitude and length scale can be analyzed.[24] Group III–V semiconductor alloys of interest for solid-state lighting, for example, show a tendency to phase separate; nanowires provide access to new composition regimes,[25] and APT can, in principle, be used to follow alloy decomposition. Finally, nanowire heterojunctions,[26] whether axial or radial (core-shell), are compelling targets because transmission measurements do not distinguish between flat-graded interfaces and chemically abrupt but curved interfaces.[27,28]

Specimen preparation for APT analysis of nanowires differ in some important respects from that of bulk specimens; the sample requirements specific to nanowires are summarized briefly before considering the results of APT analysis. Nanowires of ~30 nm diameter and greater can be manipulated and mounted on micropost arrays using approaches similar to those discussed in the section on "Metrology Challenges in Highly Scaled Semiconductors," but nanowires may also be grown "in place" on posts,[29] Figure 1b. To adopt this latter approach, the density of nanowires needs to be well controlled, such that ions from only one nanowire are collected. The first demonstration of APT on a nanowire was performed using voltage pulsing of InAs nanowires grown on GaAs(111)B substrates.[30] Subsequent studies have found that the yields are much higher for pulsed-laser operation for at least two reasons.[29] First, the cyclic mechanical stresses associated with hydrostatic strain induced by voltage pulsing are absent. Second, laser pulsing enables analysis of less conducting materials at lower voltages. Laser pulsing with a green laser (532 nm wavelength), however, involves laser-beam heating and requires that the specimen return to the base cryogenic temperature in between pulses. The tip temperature also must be kept sufficiently low so that the microstructure is not affected by diffusion. The low thermal conductivity of nanowires imposes some constraints in this regard that have been described in detail in the literature.[31]

Later, we present two examples of nanowire compositional characterization uniquely enabled by APT: 3D dopant distribution and heterojunction analysis. These characteristics obviously depend on how the nanowires are grown. The most prevalent approach to nanowire growth is the vapor-liquid-solid (VLS) process, whereby metal nanoparticles, most often gold, are used to seed nanowire growth through the formation of an eutectic liquid droplet with the semiconductor in question.[32] VLS growth is commonly performed in the context of CVD under conditions that otherwise might result in the more familiar thin-film growth. In this case, the nanoparticle induces preferential precursor decomposition and preferential atomic incorporation at the liquid-solid interface. Silicon and germanium are good model systems for VLS nanowire growth because the decomposition kinetics of the SiH_4 and GeH_4 CVD precursors are well matched to the eutectic temperatures of Au-Si and Au-Ge. Figure 5 displays the reconstruction of a phosphorous-doped germanium nanowire grown with a gold nanoparticle. The catalyst is visible, Figure 5a, as are atomic planes perpendicular to the ⟨111⟩ growth direction, Figure 5b. The doping rate, which is not generally known, is determined by the rate at which the dopant atoms move from the gas phase as precursors to the solid phase as substitutional impurities. Quantitative analysis of the mass spectrum from a nanowire, Figure 5, showed that the dopant concentration in the VLS-grown nanowire was much less than that of the gas phase. Furthermore, uncatalyzed reactions on the nanowire surface introduced dopants at a different rate, leading to the radial variation in doping level seen in the end-view of Figure 5c.

Radial composition gradients also can be introduced intentionally. Radial core-

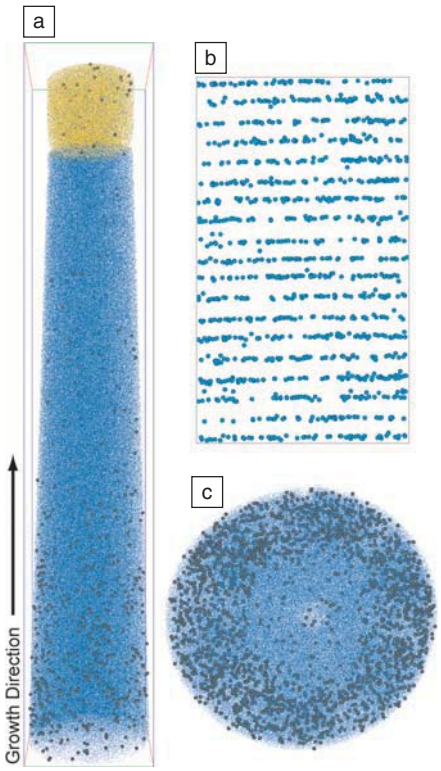

Figure 5. Three-dimensional reconstruction of doped Ge nanowire showing Au, Ge, and P atoms as gold dots, blue dots, and gray spheres, respectively. (a) Side view of an Au catalyst tip and nanowires. Arrow indicates growth direction. (b) Side view of a center portion showing (111) planes perpendicular to growth axis. (c) End-view showing a radially nonuniform doping profile due to surface growth. Adapted from Reference 33.

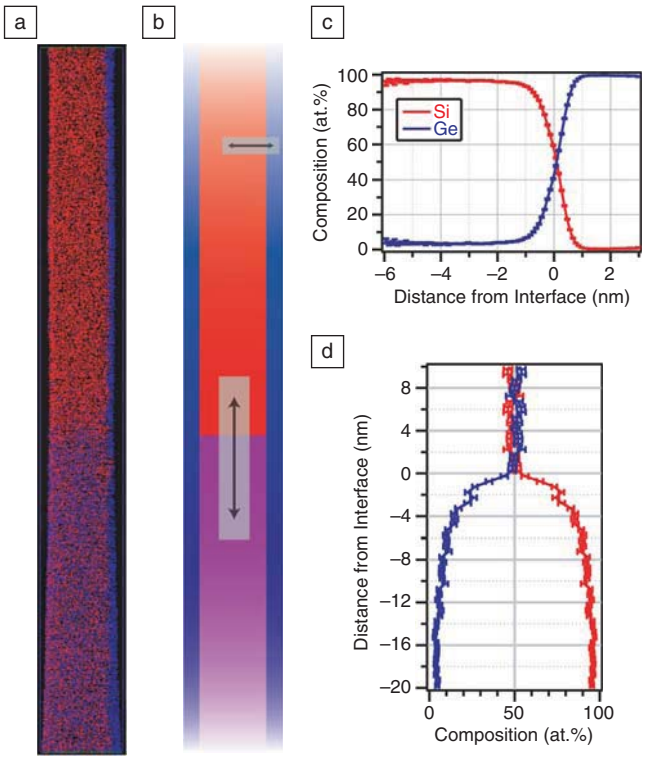

Figure 6. Atom-probe tomography reconstructions of axial and core-shell heterostructures with Si and Ge atoms as red and blue dots, respectively. (a) SiGe-Si axial heterostructure coated with Ge shell. (b) Schematic of structure. Shaded areas with arrows show regions plotted in (c) and (d). (c) Radial composition profile showing slightly diffuse Si-Ge interface. (d) Axial composition profile showing non-abrupt heterojunction. Adapted from Reference 31.

shell heterostructures,[28] in which an epitaxial shell of one material is grown around a core nanowire of another material, are of interest not only for advanced electronic and photonic devices but also for APT analysis and correlated microscopy. An APT reconstruction and analysis of a combined core-shell and axial heterostructure is shown in Figure 6. A conformal Ge shell was deposited following growth of a SiGe-Si nanowire heterostructure. The radial concentration plot in Figure 6c was extracted by a proximity histogram (explained in the section on "Silicide Contacts to Silicon"), taking the 50 at.% Si isoconcentration surface as the Si-Ge interface. Figure 6d shows an axial heterojunction with an interface perpendicular to the analysis direction. The transition between the SiGe and Si segments is not abrupt due to the fact that Ge is dissolved in the gold catalyst and does not immediately deplete when the source gas is switched off. More abrupt junctions, which are generally desirable for electronic and photonic devices, might be obtained by using catalyst particles that remain solid at the growth temperature. Unlike conventional STEM, APT can discriminate between a junction that is abrupt but nonplanar and one that is planar but diffuse, thereby providing critical feedback on approaches to heterojunction formation. While interface abruptness is of intrinsic and practical interest, the presence of a shell facilitates analysis of other characteristics. First, the shell decreases the magnification by increasing the tip radius a specified amount, projecting the entire Si nanowire core within the field of view of the 80-mm diameter detector through the controlled increase of the specimen radius. Second, the shell serves as a marker of the Si nanowire surface for investigations of surface doping or surface segregation during growth. Third, the absolute diameter of the core is readily determined by correlating with TEM and STEM characterization, leading to a quantitative APT reconstruction in the radial direction. Core-shell nanowire samples should also prove useful in efforts to correlate STEM-based tomography, which provides atomic resolution, with APT, which provides single-atom chemical sensitivity.

Summary

This brief review has identified important contributions of atom-probe tomography (APT) to the development of semiconductor materials and devices based on the unique atomic-scale chemical information that the technique can provide. Work on transition metal alloyed nickel silicides illustrates the capability to engineer phase formation and control the morphology and microstructure of the source and drain contacts. High sensitivity and high spatial resolution impurity distribution profiling in 3D in a pFET device structure highlights how APT, in conjunction with electrical characterization, can uniquely aid in the design of future devices and help in failure analysis. APT has shown distinctive capability to characterize nanowire heterostructures, providing excellent information on impurity distributions in 3D as well as heterojunction abruptness, thus tackling

questions of both scientific and technological importance. Additional promising applications include other device structures, such as light-emitting quantum wells,[19] photovoltaic materials,[34] and quantum dots. We anticipate that APT will play an essential and expanding role in the continuing development of semiconductor materials, devices, and technologies.

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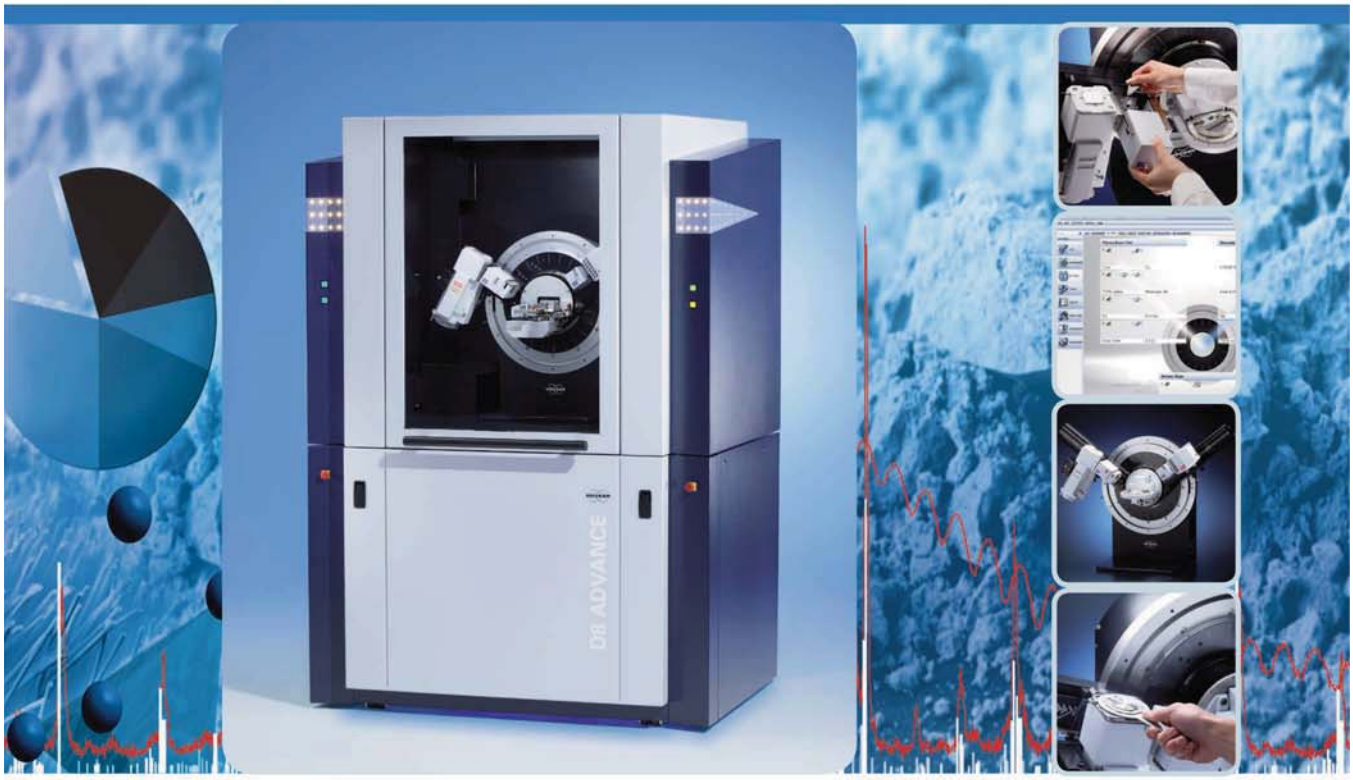

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